CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent Office, number 1-571-273-8300, or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope, or filed electronically and addressed to: Mail Stop AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 9, 2006.

Gerardo Ubau

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/821,505	Confirmation No. 9848
Applicant	:	Steve C. Huang	
Filed	:	April 9, 2004	
TC/A.U.	:	2825	
Examiner	:	Sun J. Lin	
Docket No.	:	ID-04-01	
Customer No.	:	30349	

Title: METHOD AND SYSTEM FOR PROVIDING FAST DESIGN FOR TESTABILITY PROTOTYPING IN INTEGRATED CIRCUIT DESIGNS

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Notice of Non-Compliant Amendment mailed **April 4, 2006**, and in response to the Office action of **January 23, 2006**, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 11 of this paper.

An **Appendix** including amended drawing figures is attached following page 13 of this paper.

Amendments to the Specification:

Please replace the paragraph on page 32 with the following paragraph:

Method and system for providing a computer implemented process of performing design for testability analysis and synthesis in an integrated circuit design includes partitioning each logic block in an integrated circuit design based on one or more boundaries of multi-cycle initial setup sequence, excluding one or more partitioned logic blocks with multi-cycle initial setup sequence from valid candidate blocks, selecting a constraint setting set, extracting a subset of constraint settings from the selected constraint setting set, applying the extracted subset of constraint settings to the integrated circuit design, performing design for testability analysis and synthesis on the valid candidate blocks, performing scan cell replacement. The scan cell replacement may include performing class selection from a cell library and a gate-level netlist based on affinity between cells, determining a target characterization, such as timing, power, area, for example, for the scan cell replacement, and replacing one or more cells with a corresponding one or more scan cells having the closest target characteristics.